FIG. 1
PRIOR ART

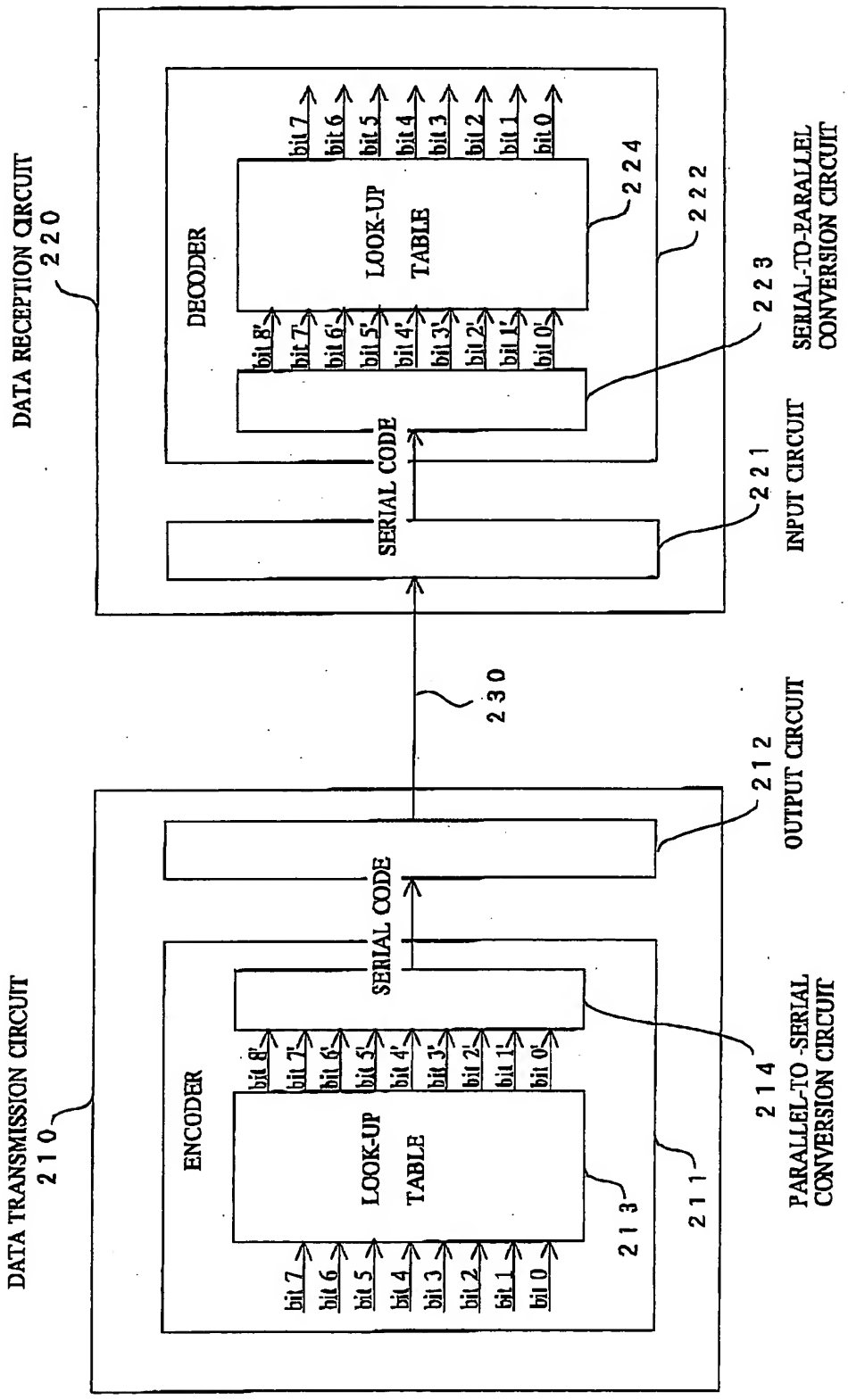


FIG. 2

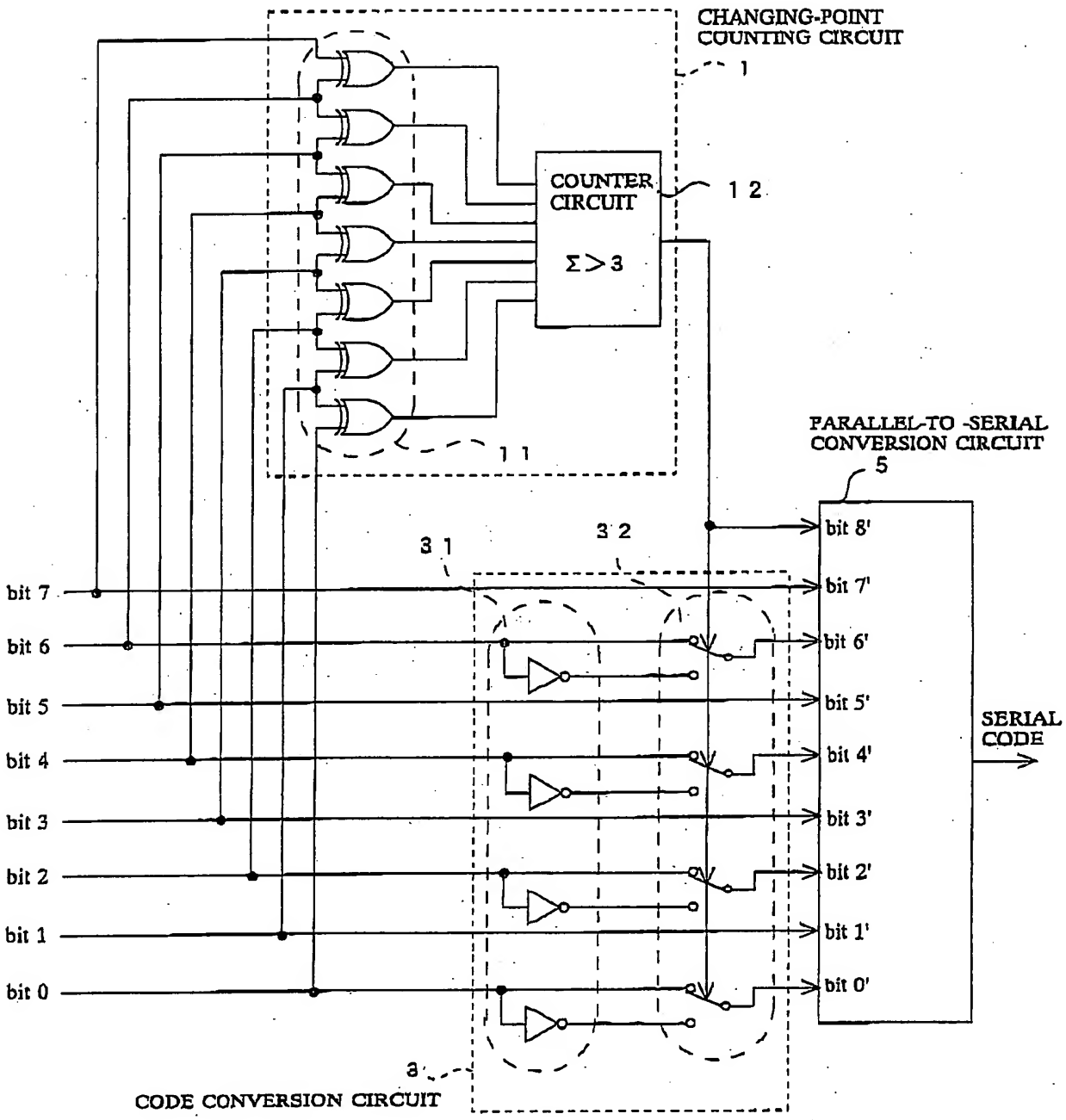

CHANGING-POINT COUNTING CIRCUIT
1
COUNTER CIRCUIT
Σ>3
12
11
PARALLEL-TO-SERIAL CONVERSION CIRCUIT
5
31
32
bit 7
bit 6
bit 5
bit 4
bit 3
bit 2
bit 1
bit 0
bit 8'
bit 7'
bit 6'
bit 5'
bit 4'
bit 3'
bit 2'
bit 1'
bit 0'
SERIAL CODE
3
CODE CONVERSION CIRCUIT

FIG. 3A

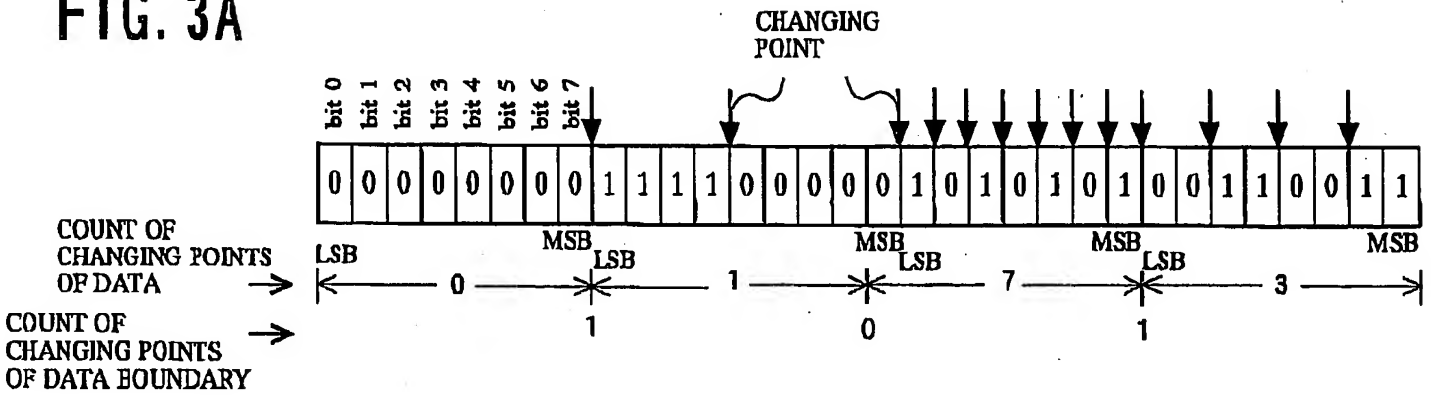

CHANGING POINT
bit 0
bit 1
bit 2
bit 3
bit 4
bit 5
bit 6
bit 7
0 0 0 0 0 0 0 0 1 1 1 1 0 0 0 0 0 1 0 1 0 1 0 1 0 0 1 1 0 0 1 1
COUNT OF CHANGING POINTS OF DATA
LSB
MSB
LSB
MSB
LSB
MSB
LSB
MSB
0
1
7
3
COUNT OF CHANGING POINTS OF DATA BOUNDARY
1
0
1

FIG. 3B

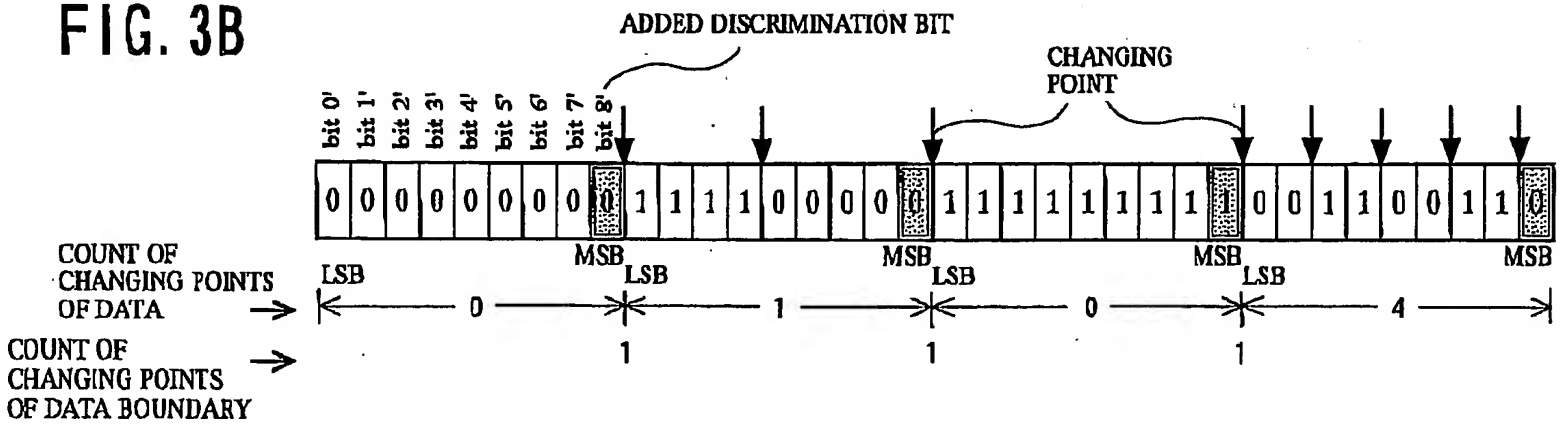
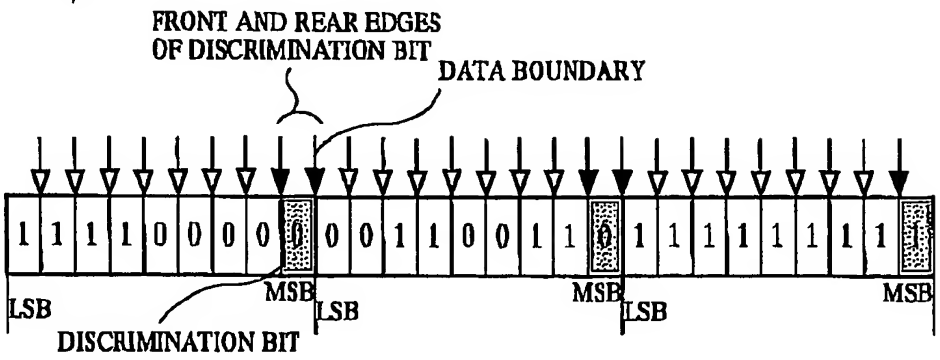

ADDED DISCRIMINATION BIT
CHANGING POINT
bit 0'
bit 1'
bit 2'
bit 3'
bit 4'
bit 5'
bit 6'
bit 7'
bit 8'
0 0 0 0 0 0 0 0 0 1 1 1 1 0 0 0 0 0 1 1 1 1 1 1 1 1 1 0 0 1 1 0 0 1 1 0
COUNT OF CHANGING POINTS OF DATA
LSB
MSB
LSB
MSB
LSB
MSB
LSB
MSB
0
1
0
4
COUNT OF CHANGING POINTS OF DATA BOUNDARY
1
1
1

FIG. 4A

DISCRIMINATION BIT IS PLACED AT MSB

: UNCONTROLLABLE CHANING POINT (PROBABILITY: 50%)

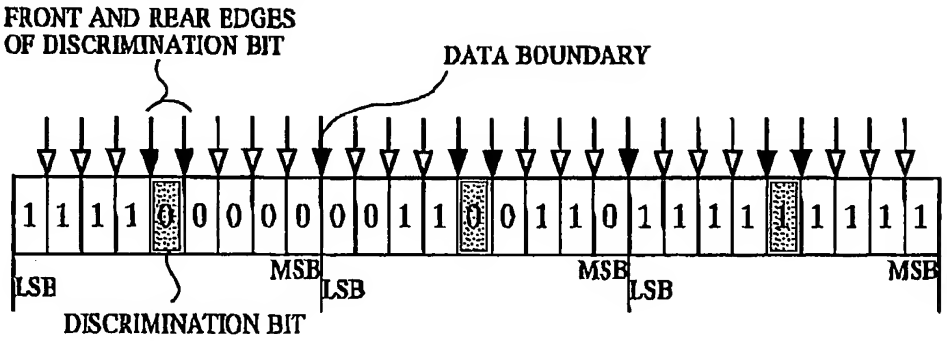
: CONTROLLABLE POINT (PROBABILITY: LESS THAN 50%)



<UNCONTROLLABLE CHANGING POINTS ARE LOCATED BEFORE AND AFTER DISCRIMINATION BIT AND AT DATA BOUNDARIES.>

FIG. 4B

DISCRIMINATION BIT IS PLACED AT OTHER THAN MSB AND LSB



<UNCONTROLLABLE CHANGING POINTS INCREASE.>

FIG. 5

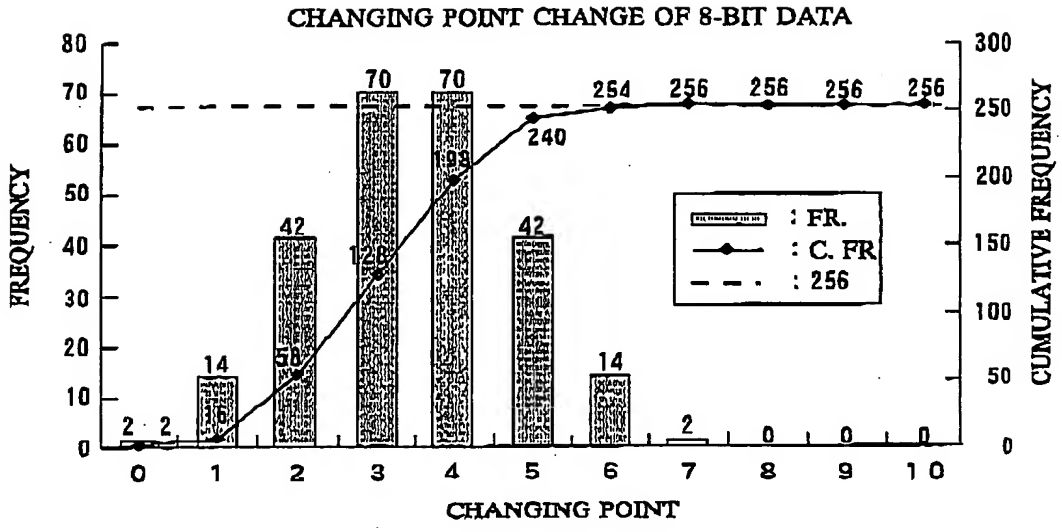

CHANGING POINT CHANGE OF 8-BIT DATA
FREQUENCY
CUMULATIVE FREQUENCY
CHANGING POINT
: FR.
: C. FR
: 256
2
2
14
42
70
70
42
14
2
0
0
0
254
256
256
256
256
240

FIG. 6

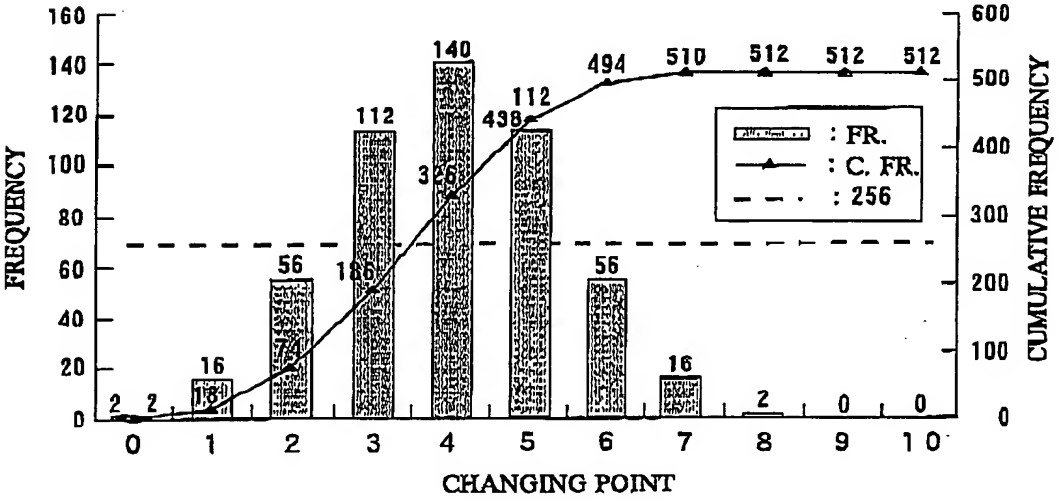

CHANGING POINT CHANGE OF 9-BIT DATA
FREQUENCY
CUMULATIVE FREQUENCY
CHANGING POINT
: FR.
: C. FR.
: 256
2
2
16
56
112
140
112
56
16
2
0
0
494
510
512
512
512
438
326
186

FIG. 7

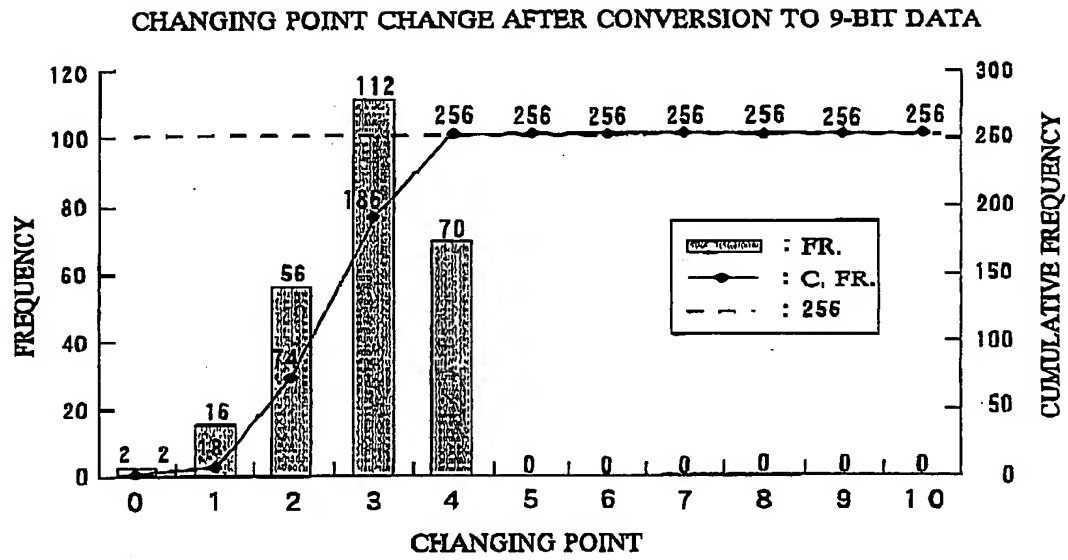

CHANGING POINT CHANGE AFTER CONVERSION TO 9-BIT DATA
FREQUENCY
CUMULATIVE FREQUENCY
CHANGING POINT
: FR.
: C. FR.
: 256
2
2
16
56
112
70
256
0
120
100
80
60
40
20
300
250
200
150
100
50
0
1 0

FIG. 8

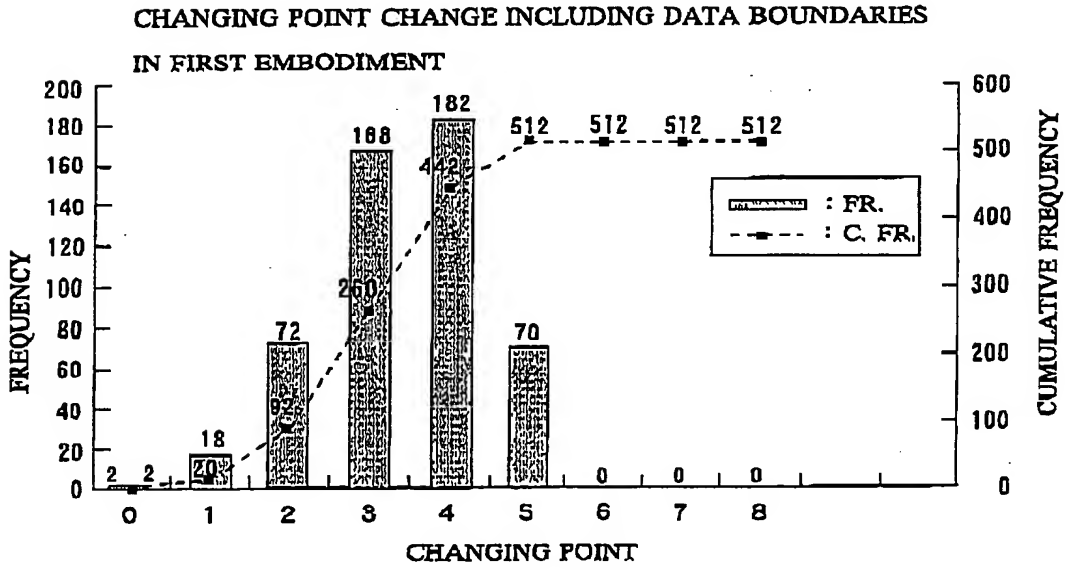

CHANGING POINT CHANGE INCLUDING DATA BOUNDARIES
IN FIRST EMBODIMENT
FREQUENCY
CUMULATIVE FREQUENCY
CHANGING POINT
: FR.
: C. FR.
2
2
18
72
168
182
70
512
0
200
180
160
140
120
100
80
60
40
20
600
500
400
300
200
100

FIG. 9

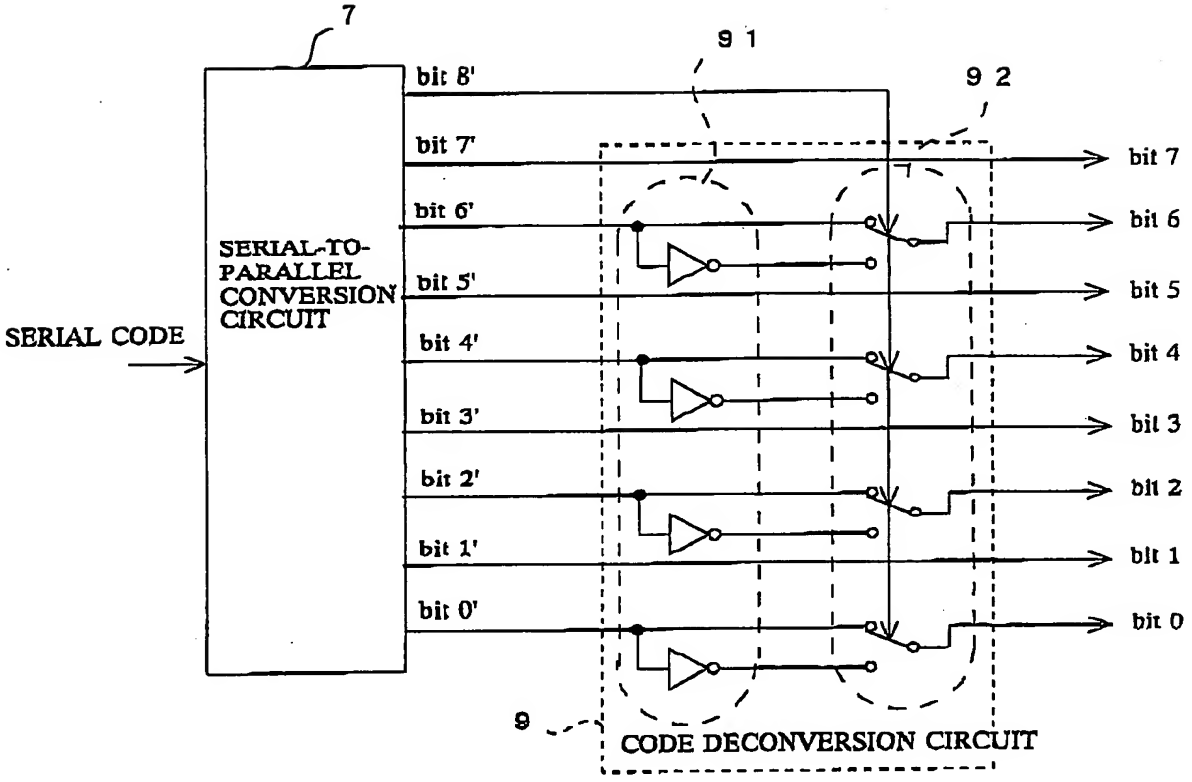

7
9 1
9 2
bit 8'
bit 7'
bit 6'
bit 5'
bit 4'
bit 3'
bit 2'
bit 1'
bit 0'
SERIAL-TO-PARALLEL CONVERSION CIRCUIT
SERIAL CODE
bit 7
bit 6
bit 5
bit 4
bit 3
bit 2
bit 1
bit 0
9
CODE DECONVERSION CIRCUIT

FIG. 10

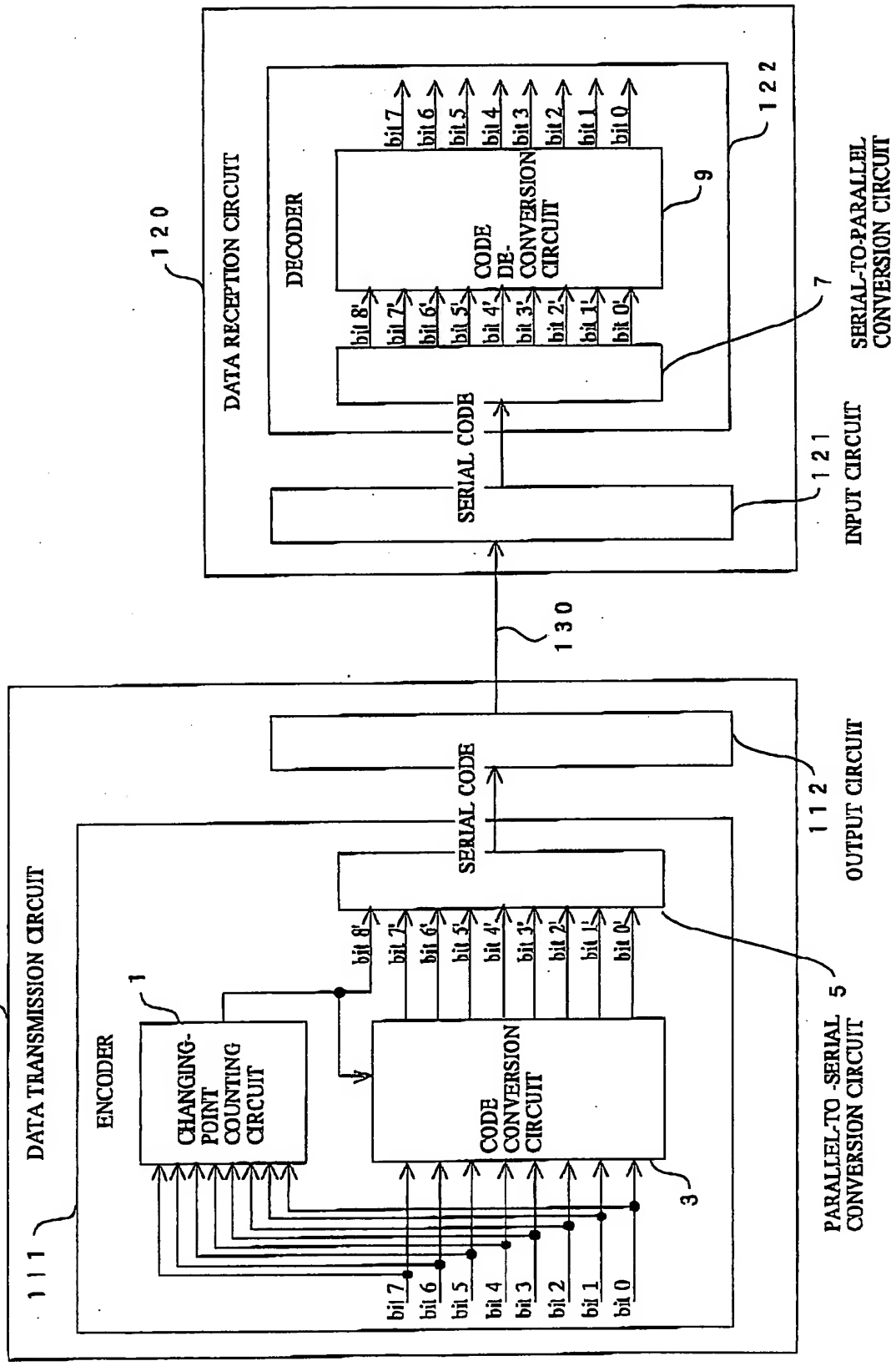

110
DATA TRANSMISSION CIRCUIT
111
ENCODER
1
CHANGING-POINT COUNTING CIRCUIT
CODE CONVERSION CIRCUIT
3
bit 8'
bit 7'
bit 6'
bit 5'
bit 4'
bit 3'
bit 2'
bit 1'
bit 0'
bit 7
bit 6
bit 5
bit 4
bit 3
bit 2
bit 1
bit 0
SERIAL CODE
5
PARALLEL-TO-SERIAL CONVERSION CIRCUIT
112
OUTPUT CIRCUIT
130
120
DATA RECEPTION CIRCUIT
121
INPUT CIRCUIT
7
SERIAL CODE
DECODER
122
CODE DE-CONVERSION CIRCUIT
9
SERIAL-TO-PARALLEL CONVERSION CIRCUIT

FIG. 11

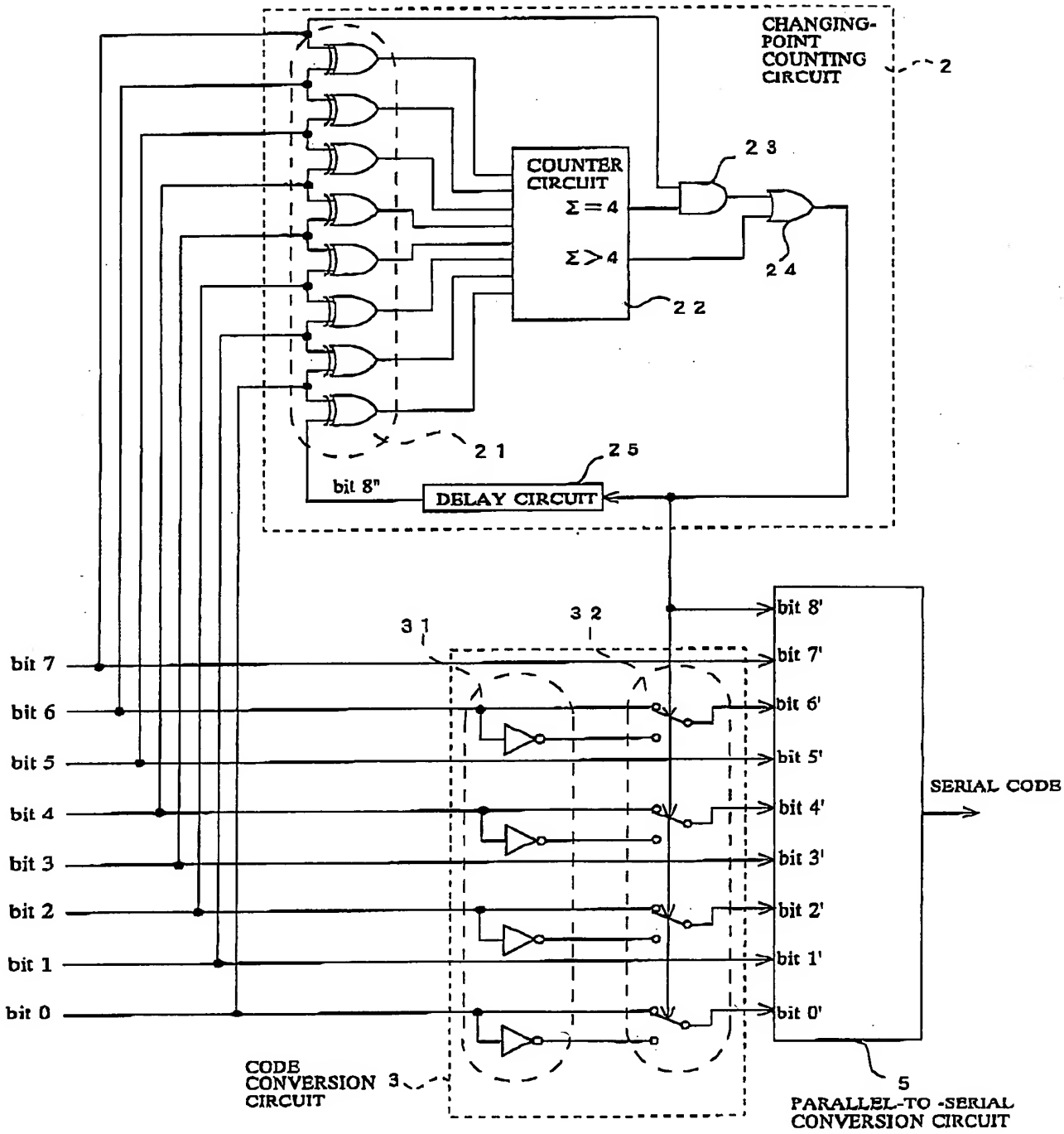

CHANGING-POINT COUNTING CIRCUIT
2
COUNTER CIRCUIT
Σ=4
Σ>4
23
24
22
21
25
bit 8"
DELAY CIRCUIT
bit 7
bit 6
bit 5
bit 4
bit 3
bit 2
bit 1
bit 0
31
32
bit 8'
bit 7'
bit 6'
bit 5'
bit 4'
bit 3'
bit 2'
bit 1'
bit 0'
SERIAL CODE
CODE CONVERSION CIRCUIT
3
5
PARALLEL-TO -SERIAL CONVERSION CIRCUIT

FIG. 12A

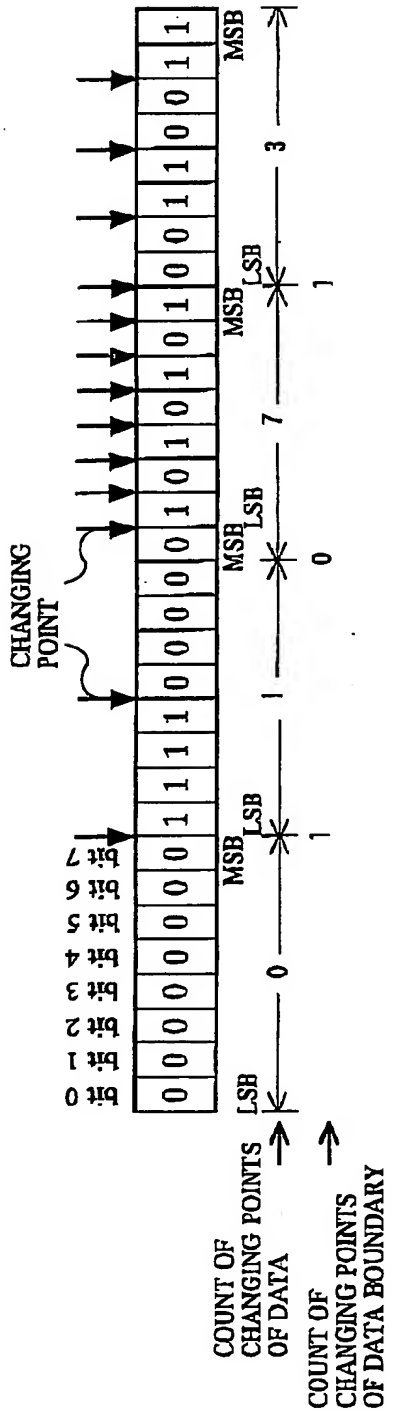


FIG. 12B

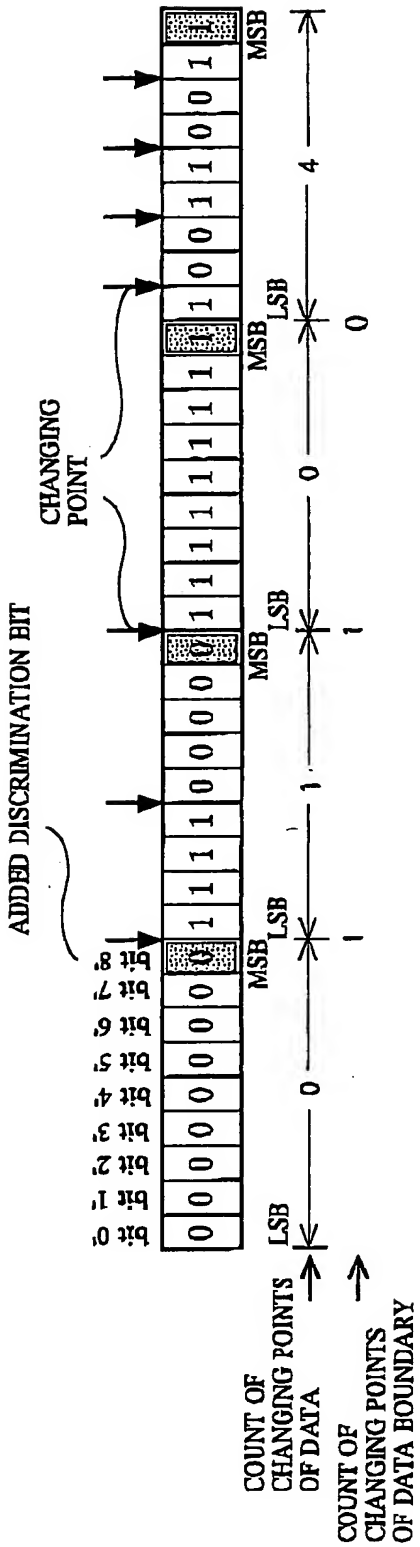


FIG. 13

CHANGING POINT CHANGE INCLUDING DATA BOUNDARIES IN FOURTH EMBODIMENT

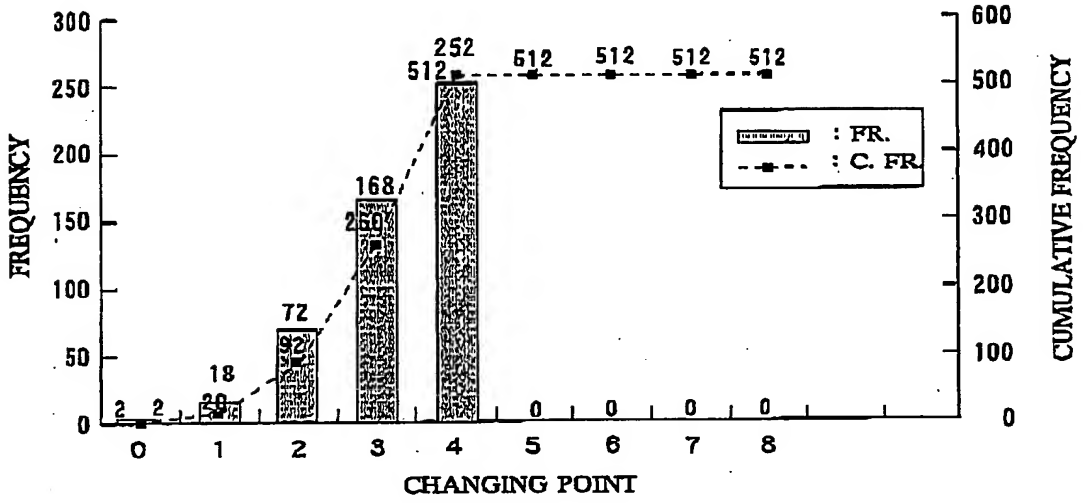


FIG. 14

CHANGING POINT CHANGE OF 10-BIT DATA

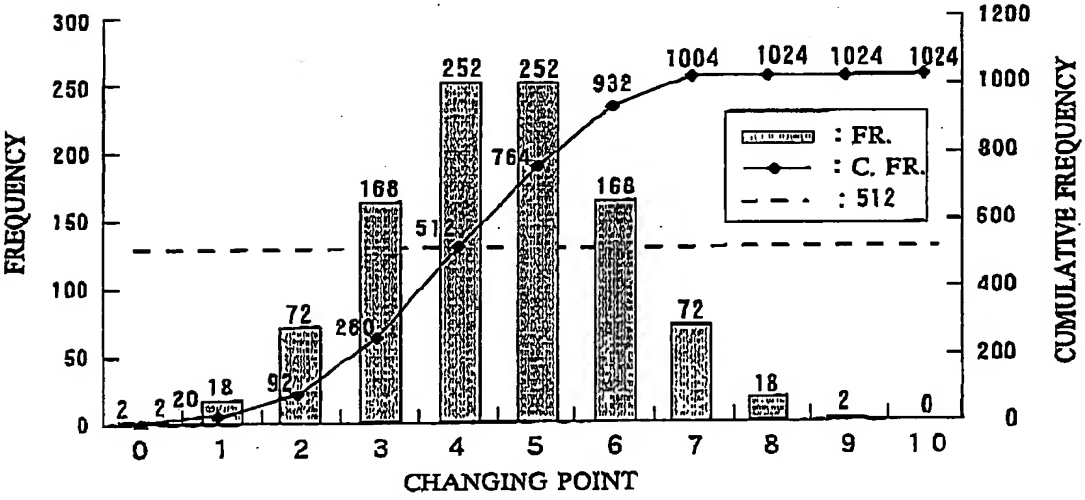


FIG. 15

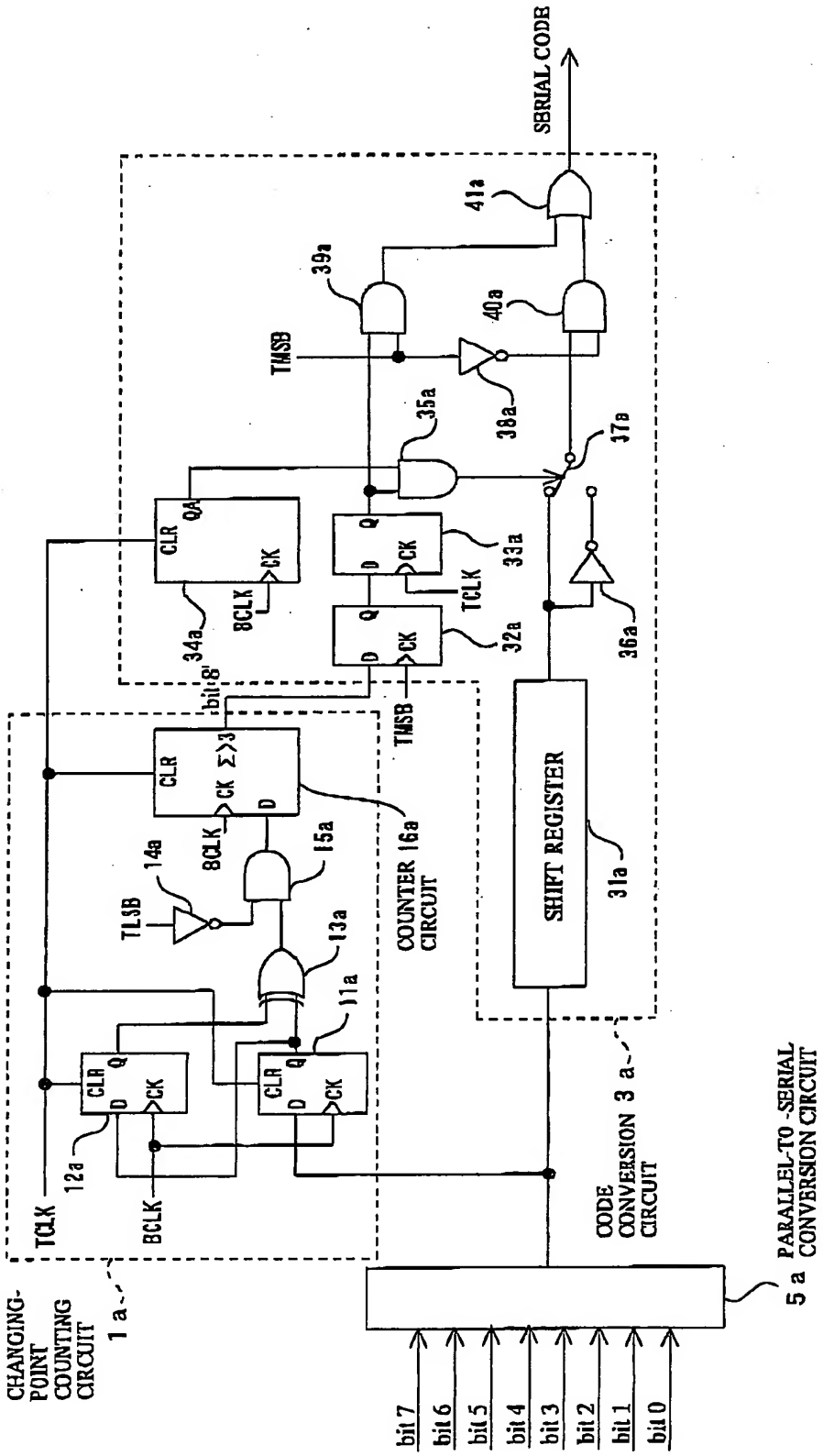

CHANGING-POINT COUNTING CIRCUIT
1a
TCLK
BCLK
12a
11a
13a
14a
TLSB
15a
BCLK
CLR
CK Σ>3
D
COUNTER 16a CIRCUIT
bit 8
TMSB
CLR
QA
CK
34a
BCLK
CLR
D
Q
CK
32a
TCLK
33a
35a
TMSB
39a
38a
40a
41a
SERIAL CODE
17a
36a
SHIFT REGISTER
31a
CODE CONVERSION CIRCUIT
3a
5a
PARALLEL-TO-SERIAL CONVERSION CIRCUIT
bit 7
bit 6
bit 5
bit 4
bit 3
bit 2
bit 1
bit 0

FIG. 16

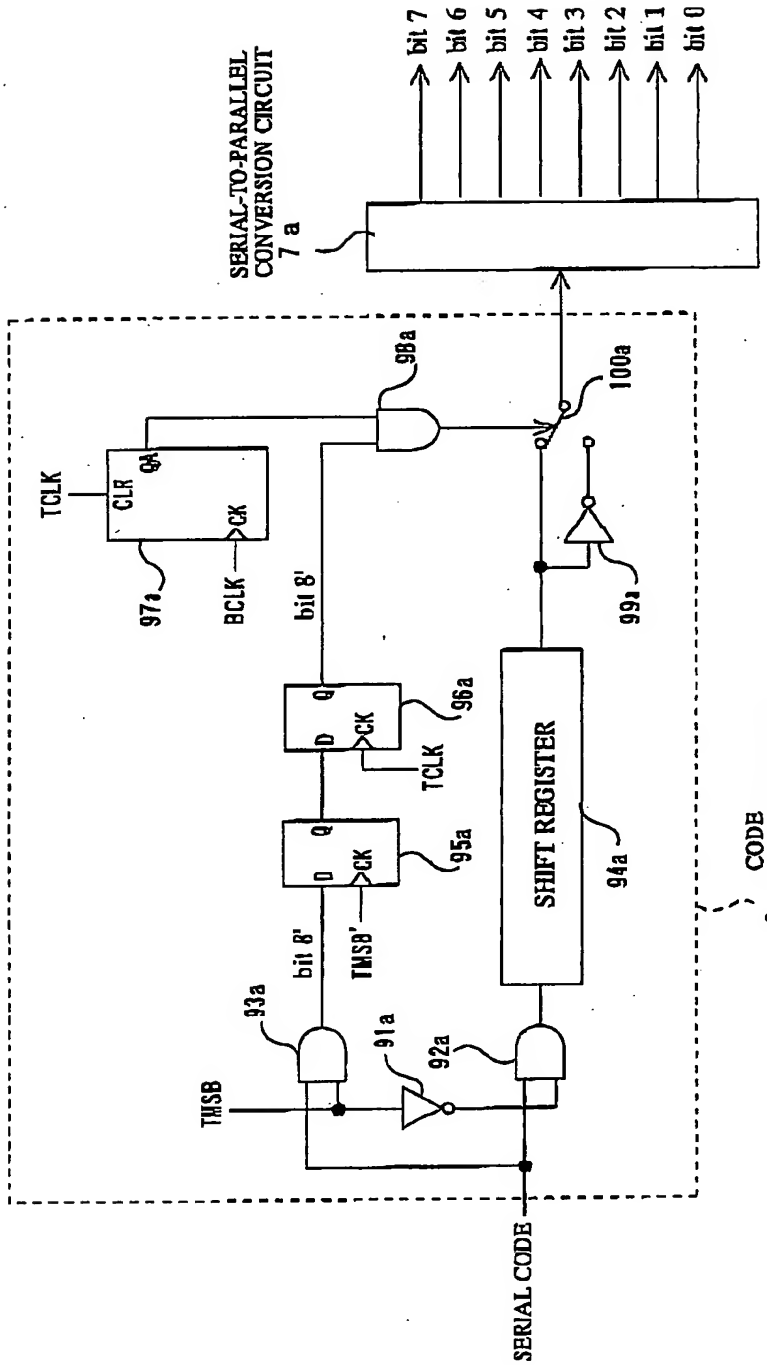

SERIAL-TO-PARALLEL CONVERSION CIRCUIT 7a
bit 7
bit 6
bit 5
bit 4
bit 3
bit 2
bit 1
bit 0
98a
100a
TCLK
CLR
Q
CK
97a
BCLK
bit 8'
99a
96a
D
Q
CK
TCLK
95a
D
Q
CK
SHIFT REGISTER
94a
bit 8'
TMSB'
93a
91a
92a
TMSB
CODE DECONVERSION CIRCUIT 9a
SERIAL CODE

FIG. 17

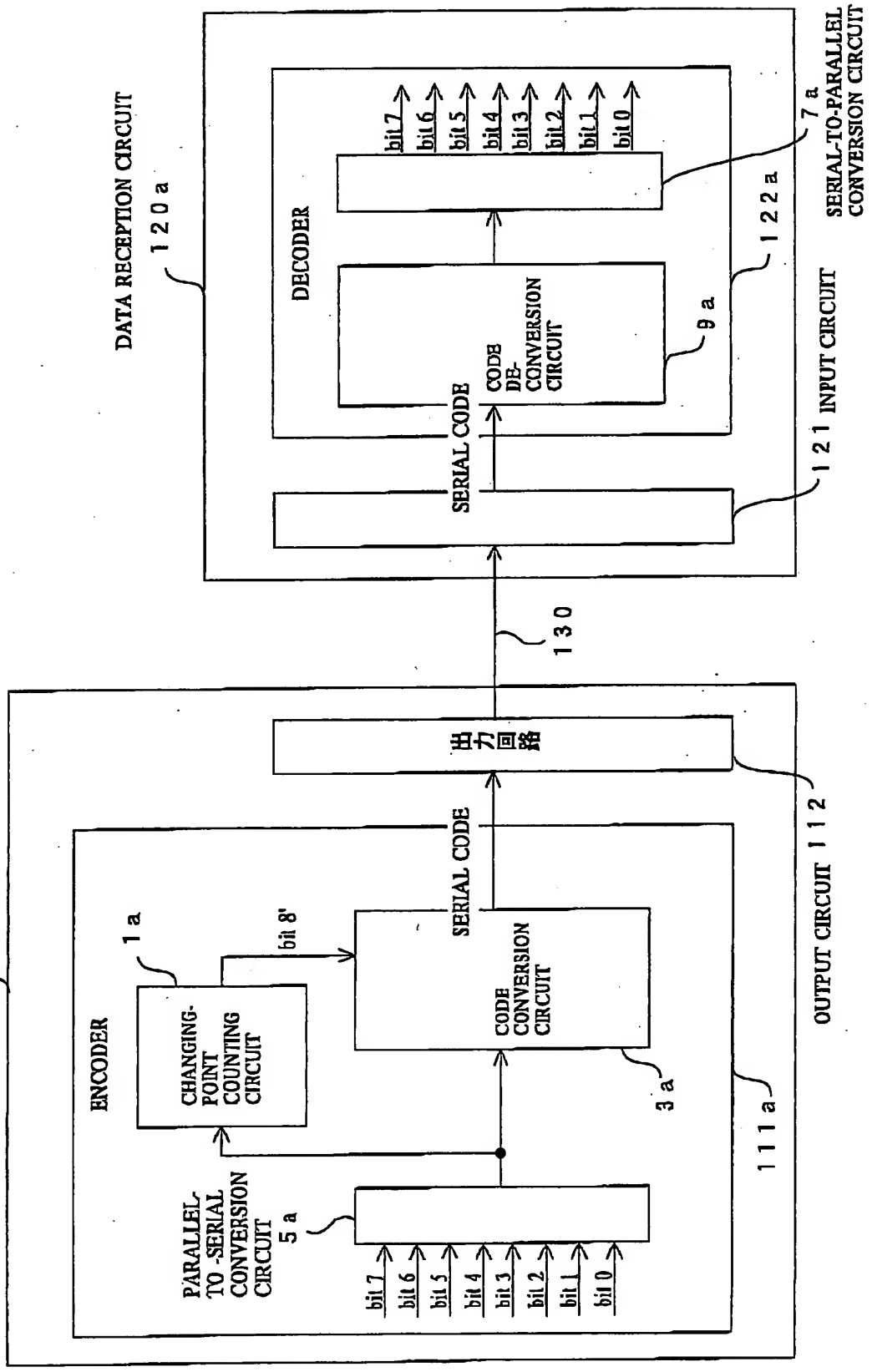

DATA TRANSMISSION CIRCUIT
110a
ENCODER
1a
CHANGING-POINT COUNTING CIRCUIT
bit 8'
PARALLEL-TO-SERIAL CONVERSION CIRCUIT
5a
bit 7
bit 6
bit 5
bit 4
bit 3
bit 2
bit 1
bit 0
SERIAL CODE
CODE CONVERSION CIRCUIT
3a
111a
出力回路
OUTPUT CIRCUIT 112
130
DATA RECEPTION CIRCUIT
120a
121 INPUT CIRCUIT
SERIAL CODE
CODE DE-CONVERSION CIRCUIT
9a
DECODER
122a
7a
SERIAL-TO-PARALLEL CONVERSION CIRCUIT

FIG. 18

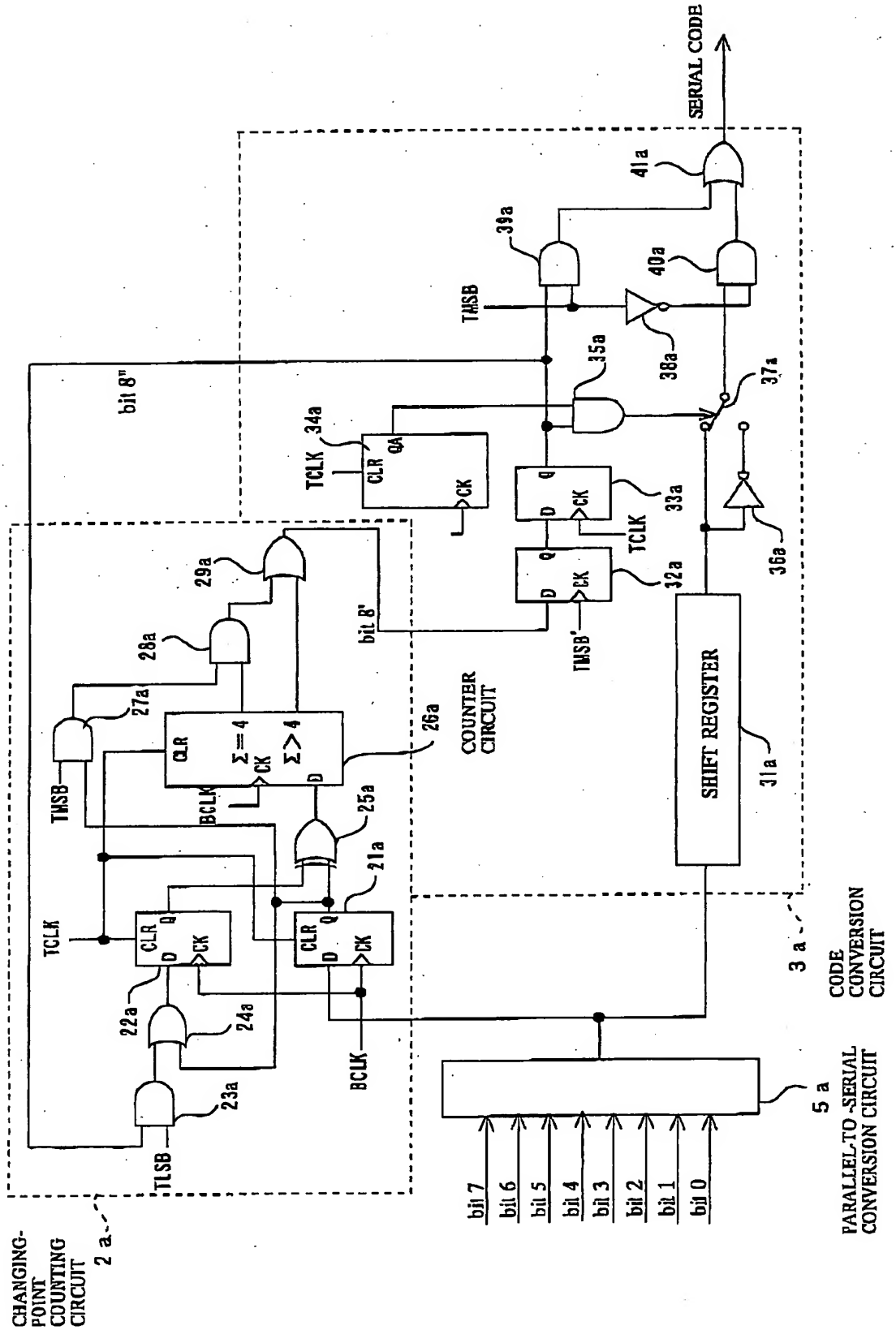
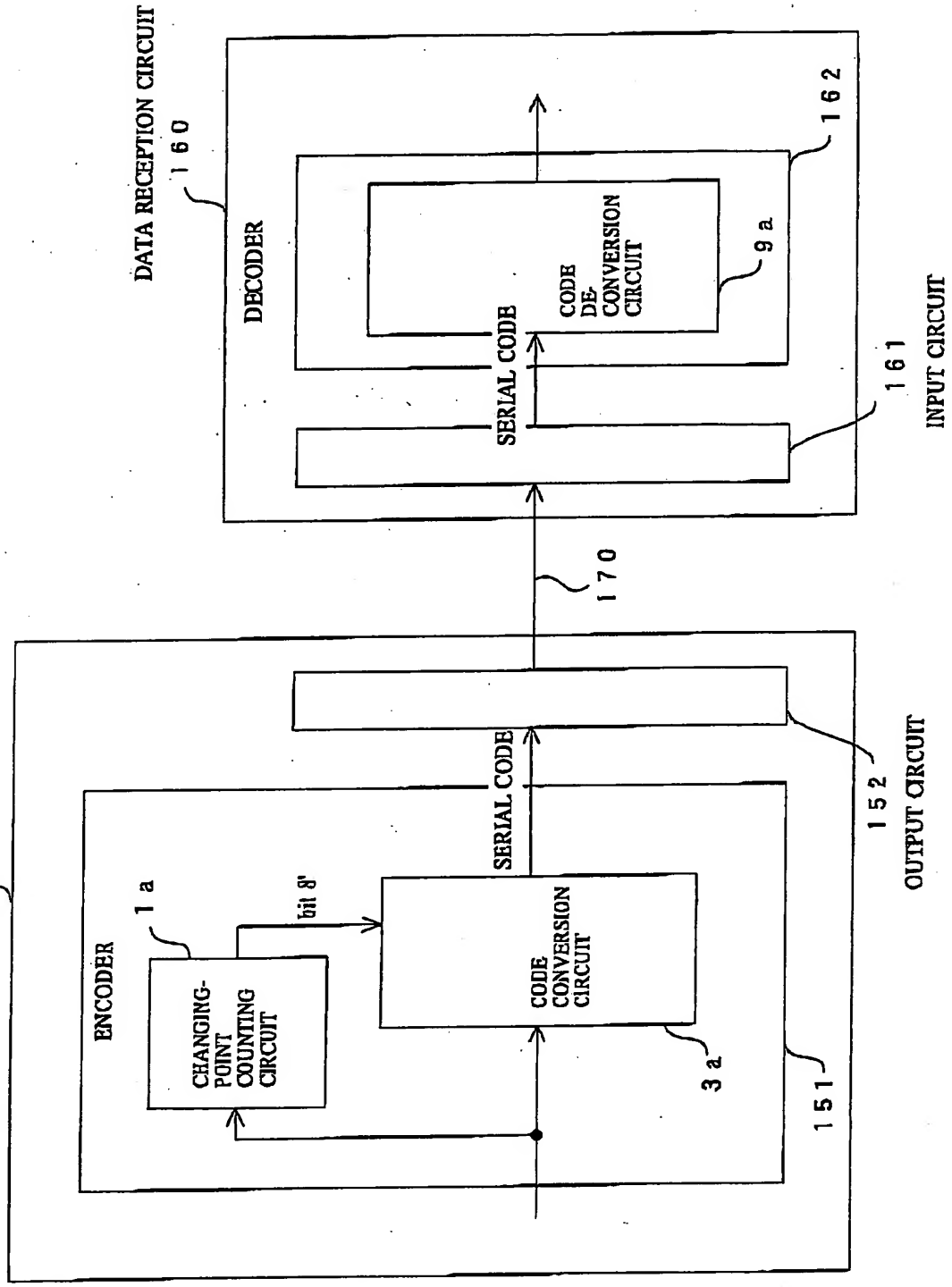

SERIAL CODE
41a
39a
40a
TMSB
38a
35a
37a
bit 8"
TCLK
34a
CLR
QA
CK
33a
D
Q
CK
TCLK
36a
32a
D
Q
CK
TMSB'
bit 8'
29a
28a
27a
26a
CLR
Σ=4
Σ>4
CK
D
BCLK
25a
21a
TMSB
TCLK
CLR
Q
D
CK
22a
24a
23a
TLSB
BCLK
COUNTER CIRCUIT
SHIFT REGISTER
31a
3a
CODE CONVERSION CIRCUIT
bit 7
bit 6
bit 5
bit 4
bit 3
bit 2
bit 1
bit 0
5a
PARALLEL-TO-SERIAL CONVERSION CIRCUIT
CHANGING-POINT COUNTING CIRCUIT
2a

FIG. 19


DATA TRANSMISSION CIRCUIT
150
ENCODER
1a
CHANGING-POINT COUNTING CIRCUIT
bit 8'
CODE CONVERSION CIRCUIT
3a
SERIAL CODE
151
152
OUTPUT CIRCUIT
170
DATA RECEPTION CIRCUIT
160
DECODER
161
INPUT CIRCUIT
SERIAL CODE
CODE DE-CONVERSION CIRCUIT
9a
162